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EXAMINER	
WOODS, ERIC V	
ART UNIT	**PAPER NUMBER**
2672	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,087	WASSERMAN ET AL.	
	Examiner	Art Unit	
	Eric V. Woods	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,13-17,20-28,30 and 32-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-17,20 and 39-41* is/are allowed.

6)☒ Claim(s) *1-10,13,20-27,30,32-41* is/are rejected.

7)☒ Claim(s) *28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-6, 8, 13-14, 20, 22, 25, 27, 33, 35, and 38 have been amended.

Claims 11-12, 18-19, 29, and 31 have been canceled.

Claims 39-41 have been added.

Response to Arguments

Applicant's arguments, see Remarks page 1, filed 21 June 2005, with respect to the rejection(s) of claim(s) 1-9 under 35 U.S.C. 103(a) have been fully considered and are persuasive.

All rejections against claims 11-12, 18-19, 29, and 31 are withdrawn since these claims have been canceled.

Therefore, the rejection of claims 1-7, 21-28, 30, and 34-38 under 35 U.S.C. 103(a) has been withdrawn in view of applicant's amendments.

The rejections of claims 1-38 under 35 U.S.C. 112, first paragraph and second paragraph, are withdrawn in view of applicant's arguments as of Remarks pages 1 and 2, which are found to be persuasive.

The objections to claims 8-10, 13-17, and 20 are withdrawn, since they have been made independent.

The objection to claim 28 is not withdrawn.

However, there are certain issues regarding claims 8-10 and 13 that must be corrected before they can be allowed (issues raised by amendment, addition of extra

means language). The addition of these rejections was **necessitated by amendment** and is **not** grounds for petition under 37 CFR 1.181.

However, upon further consideration, a new ground(s) of rejection is made in view of various references as below.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the means listed in claims 8-10 and 13 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification is objected to because it does not illustrate the means for claims 8-10 and 13. Applicant must illustrate these limitations or else cancel the claimed subject matter. Applicant further must amend without adding new matter as noted above.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claims 8-10 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, claims 8-10 and 13 recite 'means' without this means ever being defined in the specification. Applicant cannot seek protection under 35 U.S.C. 112, sixth paragraph, without pointing out and distinctly claiming the means and functions in the drawings and the specification.

Allowable Subject Matter

Claims 14-17 and 20 are allowed, as per the Reasons in the previous Office Action, since the rejections of the claims under 35 U.S.C. 112 have been withdrawn and they have been made independent with the limitations from the intervening claims.

Claims 39-41 are allowed for the reasons stated in Remarks page 2, wherein they are rewritten versions of dependent claims with allowable limitations and the intervening claim language.

Claim 28 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-10 and 13 would be allowable if the rejection under 35 U.S.C. 112, second paragraph, were overcome.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson (US 5,129,092) in view of Willson, Jr. et al (US 6,553,397 B2)('Wilson').

As to claim 1,

A system for generating pixels from a distributed convolution of samples comprising: (Preamble is not given patentable weight, since it only recites a summary of the claim and/or an intended use, and the process steps are capable of standing on their own; see Rowe v. Dror, 112 F.3d 473, 42 USPQ2d 1550 (Fed. Cir. 1997), Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999), and the like.)

-A plurality of sample managers connected in series; and (Wilson clearly teaches in Abstract and in Figure 1 a plurality of processor groups each comprising of individual processing elements 10a-10h, wherein each group of elements is connected to the element adjacent to it using data lines 11i-11n and register shift lines 21i-21n, as set forth in 5:55-6:34, these elements are clearly connected in series (as in 2:45-60, where it states that these elements are connected in a **linear chain**, where in Figure 1 it is clear that is input from data input device 20 over lines 21a and then passed in a one-way manner down the line on lines 21i→21n))(Willson clearly teaches a digital filter where each element generates a partial sum in Figure 5A)

-A set of partial sums buses wherein each partial sums bus connects one of the sample managers of the series to the next sample manager in the series; (The term **bus** is well known in the art to merely mean one or more data transfer lines, wherein the data lines 11i-11n and 21i-21n clearly move data in byte-size chunks, which therefore mean that they are "buses" in the sense meant by applicant. Clearly, these buses can transfer partial sums, as in 18:20-60, where it is noted that partial sums can be moved along the chain of processors)(Willson – clearly the connections between each element constitute

as sample bus, since data and control lines are clearly buses, as are the lines between each of the addition nodes on the accumulator lines, as in Figure 5A.)

-Wherein each sample manager is operable to calculate partial sums for a corresponding portion of the samples located within a convolution kernel corresponding to a pixel location, wherein the partial sums comprise 1) a sum of weights determined for locations of the samples in the portion of samples and 2) a sum of weighted sample values for the portion of samples, (Wilson is designed to process images in 8x8 bit submatrices, as in Abstract, and 2:45-3:4. Further, in 1:10-35 Wilson teaches that inherently, data arrays such as images must be broken into smaller data array sizes with dimensions equivalent to the size of the processor array. Therefore, the recited 'convolution kernel' in applicant's specification consists a certain N x N region, as noted in Remarks page 1, of which the 8x8 sub-matrix or sub-array of Wilson would clearly qualify. Clearly, the resultant element is passed down the processor line to be operated upon, which provides a sum of weighted values for that portion of samples. Further, in 18:20-60 it is clearly explained that the system is intended to handle convolutions and/or sums as part of processing images, where these can clearly be partial sums. Wilson very clearly teaches many common tasks in image filtering, such as transposes (16:40-50), accumulation (19:20-60), and the like (16:53-18:20, 18:60-19:50).)(Willson clearly teaches that the data is passed down the adder / processing element chain and that it consists of partial sums as data in 18:55-19:25. Next, Willson can be a FIR filter, where an FIR filter inherently consists of weight functions that are 'partial sums', where each tap in such a filter very clearly causes a partial sum as the outcome, see for example

1:60-2:50, where the system is generic digital filter, where the system implements FIR filtering and other applications with weighting (see particularly (2:20-2:50). Further, a generic FIR N-tap digital filter implementation is taught in 5:58-6:25, where the system of Fig. 5A is clearly explained in 7:15-67. FIR filters are well known in the art to be applied to images, and **note that Willson clearly teaches in 4:14-18 that the filters are advantageously applied to any task involving digital filters, which would prima facie include image processing.**)

-Wherein each of the second through the last sample manager in the series is operable to add the partial sums calculated for its corresponding portion of the samples to any previously accumulated partial sums received from the prior sample manager in the series, and if not the last sample manager in the series, output new accumulated partial sums to the next sample manager in the series. (Wilson clearly teaches that for the accumulator model, each group of processing elements passes the partial sums along towards the right. Clearly, the system will take the partial sums calculated for its portion of the same sample and output the results to the next group of processing elements in the series)(Willson clearly shows that the processing array passes results down the chain to be accumulated and that each partial sum element adds the results from its element and then outputs the new partial sums down the chain to the next element, as required).

Examiner contends that Wilson per se teaches the limitations of the above claim. However, in order to expedite prosecution, the Willson reference is added to explicitly cover certain details of how a chain of linearly connected accumulation elements for an

image-processing filter would operate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the systems of Wilson and Willson because the system of Willson allows for much lower power consumption during the computation of such values and a reduced number of operations (see for example Abstract, 6:50-7:15, and the like), and the system of Wilson allows for better control of certain elements of the operation of groups of linearly connected blocks containing multiple processing elements each.

As to claim 2, clearly Wilson is computing image data as noted above, so the last sample manager would clearly calculate pixel values, where the output data is clearly computed by the final element and sent out from the final unit using data line 21p to output device 22, which clearly shows that such data is image data, and the like. Further Willson teaches processing image data in Figure 2 in any case.

Claims 3, 23, 25-27, 30, 32-33, and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson in view of Willson as applied to claims 1 and 2 above, and further in view of Inada et al (US 2004/0004620 A1)('Inada').

As to claim 3, the system of claim 2, wherein for each sample manager the corresponding portion of samples resides in a sub-set of screen space and the sub-sets are finely interleaved across screen space. Clearly the system of Inada establishes in [0154] that the system breaks the screen down into blocks of 4x4 pixels for interleaving, which constitutes a distribution across screen space, and further in Fig. 1 it is shown how the screen is divided into smaller areas, where each area is analyzed for the

presence of a primitive in the pixels in that particularly, smaller area. Further, Wilson teaches the division of an image into blocks or sub-arrays for processing and convolution purposes. That being said, It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the systems of Wilson and Willson for the reasons set forth above (the motivation and combination of claim 2 are herein incorporated by reference) with the system of Inada, to allow interleaving as that technique speeds up drawing time (Inada [0155]).

As to claim 21, the rejection to claim 1 is incorporated by reference. Firstly, the claimed filter unit as recited is clearly comparable to the sample managers recited in previous claims, as the functionality is the same, and the processing element would clearly be performing similar tasks. Each of the N memories recited is attached to a group of processing elements, which serves as a filtering element / sample manager / generic processor, as set forth in Wilson Fig. 1. Clearly the system of Inada establishes in [0154] that the system breaks the screen down into blocks of 4x4 pixels for interleaving, which constitutes a distribution across screen space, and further in Fig. 1 it is shown how the screen is divided into smaller areas, where each area is analyzed for the presence of a primitive in the pixels in that particularly, smaller area, and in Fig. 7 the screen is shown to be divided into 2x2 bins or tiles containing samples for processing purposes. Further, Wilson teaches the division of an image into smaller arrays, as in Wilson is designed to process images in 8x8 bit submatrices, as in Abstract, and 2:45-3:4. Further, in 1:10-35 Wilson teaches that inherently, data arrays

such as images must be broken into smaller data array sizes with dimensions equivalent to the size of the processor array.

Next, the recited N and k can clearly be 1. Obviously, the system of Wilson has one or more memory per processing group as connected in Figure 1 – see Wilson 5:55-6:45 and shown and the system of Inada has a graphics memory 145 with a memory interface circuit 144 as shown in Fig. 2, where clearly this meets the recited limitations for the fact that N and k can be 1. Each unit of Willson is an individual tap of the filter or similar implementation. The recited numeric limitations – that of N and k, are obvious in that any chain of processors would have each processor numbered as set forth in the claim, with the respective limitations, in that, for example, the first processor in the chain would be numbered zero, and of course the first processor would *prima facie* not receive data from a previous processor as it was the first one in the processor chain.

As set forth in the preceding paragraph, each processor 10a-10h in the processing group in Wilson obviously reads from its own memory that contains the section of the image assigned to (as in Inada) for convolution purposes (or Wilson), performs partial sum calculations on it, and moves it into the next element in the linearly connected array (Wilson). The entire question of partial sums and their calculations is covered in the sections of the rejections of claim 1 that has been expressly incorporated via reference and will not be repeated for the purposes of brevity.

One additional note is that the system of Inada as shown in Fig. 4 clearly shows a plethora of operations units attached to each register (e.g. operation units 1411-1,

1412-1, etc. attached to registers such as 1411-2), which clearly establishes multiple processing / operations units attached to memories in the first place.

Obviously, the system of Inada outputs pixels as set forth in paragraphs [0022-0024]. Clearly, the results of all the graphics calculations and convolutions would be passed out as pixel data as shown there, and it is logical that the end results of an image convolution calculation from a chain would indeed be output as pixels – indeed, an image is fundamentally composed of pixels, and it is a fundamental of the digital signal processing art that an image is output in pixels from being processed in this context.

Motivation and combination is taken from the rejection to claim 1, which is incorporated by reference, and from the additional logic as set forth above. Inada brings in the benefits of explaining how the screen space is subdivided so that such an array can thusly more efficiently process all the information provided from the subdivision of the screen space. Motivation / rationale is also taken from the rejection to claim above.

As to claim 23, it is a substantial duplicate of claim 21 under the circumstances where M is 1. For other circumstances, obviously the system of Wilson can be dynamically reconfigured to support the desired arrangement of processing elements, depending on numbers of processors per group, as it could be composed of FPGAs that are fundamentally reprogrammable and/or could simply be programmed in a different manner, given that each processing group has so many processing elements. Therefore, division into groups is a trivially obvious variant. Also, Inada is **only** included

for division of screen space, which examiner contends would be a notoriously and trivially obvious variant anyway.

As to claim 25, it is merely a method implementing the system of claim 21, and the rejection to claim 21 is valid upon it without further comment.

As to claim 26, see the rejection to claim 3 above, which addresses regions having defined boundaries, wherein the screen space is divided asset forth there. Inada [0020] discusses how each region is judged with respect to its center point, which clearly establishes that this is an obvious variation. Motivation and combination are taken from the parent claim and incorporated herein by reference in their entirety.

As to claim 27, this limitation is expressly covered in the rejection of claim 1, the relevant portion of which is incorporated by reference, and is also stated below. Wilson is designed to process images in 8x8 bit submatrices, as in Abstract, and 2:45-3:4. Further, in 1:10-35 Wilson teaches that inherently, data arrays such as images must be broken into smaller data array sizes with dimensions equivalent to the size of the processor array. Therefore, the recited 'convolution kernel' in applicant's specification consists a certain N x N region, as noted in Remarks page 1, of which the 8x8 sub-matrix or sub-array of Wilson would clearly qualify. Clearly, the resultant element is passed down the processor line to be operated upon, which provides a sum of weighted values for that portion of samples. Further, in 18:20-60 it is clearly explained that the system is intended to handle convolutions and/or sums as part of processing images, where these can clearly be partial sums. Wilson very clearly teaches many common tasks in image filtering, such as transposes (16:40-50), accumulation (19:20-60), and

the like (16:53-18:20, 18:60-19:50).)(Willson clearly teaches that the data is passed down the adder / processing element chain and that it consists of partial sums as data in 18:55-19:25. Next, Willson can be a FIR filter, where an FIR filter inherently consists of weight functions that are 'partial sums', where each tap in such a filter very clearly causes a partial sum as the outcome, see for example 1:60-2:50, where the system is generic digital filter, where the system implements FIR filtering and other applications with weighting (see particularly (2:20-2:50). Further, a generic FIR N-tap digital filter implementation is taught in 5:58-6:25, where the system of Fig. 5A is clearly explained in 7:15-67. FIR filters are well known in the art to be applied to images, and **note that Willson clearly teaches in 4:14-18 that the filters are advantageously applied to any task involving digital filters, which would prima facie include image processing**.)

As to claim 30, this is an obvious variation and is addressed in the rejection to claim 21 and is repeated herein. Obviously, the system of Inada outputs pixels as set forth in paragraphs [0022-0024]. Clearly, the results of all the graphics calculations and convolutions would be passed out as pixel data as shown there, and it is logical that the end results of an image convolution calculation from a chain would indeed be output as pixels – indeed, an image is fundamentally composed of pixels, and it is a fundamental of the digital signal processing art that an image is output in pixels from being processed in this context. Motivation and combination are incorporated by reference from the parent claim.

As to claim 32, Inada clearly addresses this limitation wherein it would be obvious to divide the screen up into bins and assign each one to an FPGA or processing element or filtering element, whatever the generic terminology for the groups of Wilson or the elements of Willson.

As to claim 33, Clearly the system of Inada establishes in [0154] that the system breaks the screen down into blocks of 4x4 pixels for interleaving, which constitutes a distribution across screen space, and further in Fig. 1 it is shown how the screen is divided into smaller areas, where each area is analyzed for the presence of a primitive in the pixels in that particularly, smaller area. Further, Wilson teaches the division of an image into blocks for processing and convolution purposes. That being said, It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the systems of Wilson and Willson for the reasons set forth above (the motivation and combination of claim 2 are herein incorporated by reference) with the system of Inada, to allow interleaving as that technique speeds up drawing time (Inada [0155]).

As to claim 36, this is a trivially obvious variant of claim 30 is subject to the same rejection.

As to claim 37, this is a trivially obvious variant of claim 33 and is subject to the same rejection.

Claims 4 and 34 are rejected under 35 U.S.C. 103(a) as unpatentable over Wilson, Willson, and Inada as applied to claim 3 above, and further in view of Hsieh et al (US 6,819,321 B1).

As to claim 4, Inada clearly teaches dividing the screen into a plurality of bins but does not specifically teach sixteen sample managers and a four by four array of bins. Reference Hsieh et al teaches dividing the screen into a number of bins for two-dimensional image processing, where the number can be arbitrary, but where an example given is four bins in Figure 4 (3:28-40). Applicant has not established any criticality to the number of sample managers and/or bins, and as such the choice of an arbitrary number of 'sample managers' or processing elements and the division of the screen into some arbitrary number of bins is a matter of design choice, see In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Inada, Wilson, and Willson to use arbitrarily scaled bins as per Hsieh, since Hsieh decreases memory bandwidth required and provides numerous other benefits (see 2:20-40 and Abstract).

As to claim 34, it is identical to claim 4, and the rejection to which is incorporated by reference.

Claims 5, 7, and 37 are rejected under 35 U.S.C. 103(a) as unpatentable in view of Wilson and Willson as applied to claim 1, and further in view of Cloutier.

As to claim 5, Wilson and Willson do not expressly teach this limitation. Cloutier clearly teaches a plurality of groups of FPGAs in Figure 1, with these controllable by the

SIMD process controller. Cloutier Fig. 1 clearly illustrates a plurality of FPGAs configured in a matrix connection, all with global bus connections, and Fig. 3 illustrates similar connections between PEs on one FPGA. It is notoriously well known that an FPGA can be configured to emulate any other type of processor, e.g. the system of Wilson/Willson as noted above. Cloutier teaches that such a system works quickly and is more efficient for processing images and the like. Cloutier clearly establishes that as set forth above that each PE performs convolution based on weighted partial sum operations. Furthermore, the nature of convolution is such that once partial sums are computed, they must be acted on by other elements or processors to produce the final, desired results.

As such, examiner takes the position that explanations cited above in response to each element of the portion of the claim dealing with the computation and/or calculation of partials sums more than adequately meet all of the limitations set forth by that section of the claim. Further, any PE that received partials sums from the bus would clearly add them using the multiply-accumulate operations cited above, particularly in the case of a neural network that was being used to perform convolution, which would be obvious to do since the system of Cloutier clearly has established utility for performing both tasks, and optical character recognition (OCR), which requires convolution and pre-processing. Further, Cloutier clearly teaches the applicability of his system to image processing in 4:20-35. Cloutier 7:26-55 again, where it is well known that the partial sums must be added, and 4:20-35, where it is taught that the present embodiment is well-suited for matrix and vector addition and multiplication. More

specifically, the embodiment of Cloutier is taught to perform multiply-accumulate operations (8:50-9:15), which clearly requires that the network of processing elements perform multiply-accumulate operations per tile (with each processing element performing said operations), and in a neural network application, which provides feed-forward information (e.g. feedback) for pattern recognition and similar, multiply-accumulate operations used in the processing of an image would obviously be added and passed along, as the architecture of Cloutier as shown in Fig. 1 is such that data is passed along between elements in the additive fashion as set forth above. Also, the system performs convolution and uses partial sums, which clearly requires that the accumulated partial sums be passed to other elements. Cloutier clearly establishes in 7:26-55 that the system has many processing element, each of which computes its own partial sums for convolution purposes.

In light of all of the above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the system of Wilson/Willson with that of Cloutier, such that each FPGA emulated the system of Wilson/Willson and therefore allowed each section to handle one portion of screen space, as this parallel computation would inherently be faster since the parts would be duplicated and the net speed would increase. This is notoriously well known in the art.

As to claim 7, this is a duplicate of claim 2, the rejection to which is incorporated by reference.

As to claim 38, this is a duplicate of claim 5, the rejection to which is incorporated by reference in addition to the rejection to claim 37 above.

Claim 6 is rejected under 35 U.S.C. 103(a) as unpatentable over Wilson/Willson in view of Cloutier as applied to claim 5 above, and further in view of Hsieh.

Therefore, the rejection of claims 2 and 5 are incorporated by reference, and motivation and rationale are taken from each of them.

As to claim 2, clearly all of the processing elements in Fig. 1 and Fig. 3 of Cloutier are clearly connected via the global bus anyway, which clearly meets the requirements that all the sample manager be chained, and that the final member calculates pixel values – clearly each chip is computing pixel values from the results of the prior one – see Cloutier 7:7-67. Further, as explained above in the rejection to claim 1, the FPGAs and the PEs within each FPGA are all interconnected, and the PEs and the FPGAs can clearly be connected in a chain or serial fashion, as the very nature of an FPGA is that the blocks can be set to have any desired set of connections with bidirectional or unidirectional communications.

Reference Hsieh et al teaches dividing the screen into a number of bins for two-dimensional image processing, where the number can be arbitrary, but where an example given is four bins in Figure 4 (3:28-40). Applicant has not established any criticality to the number of sample managers and/or bins, and as such the choice of an arbitrary number of 'sample managers' or processing elements and the division of the screen into some arbitrary number of bins is a matter of design choice, see In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Inada, Wilson, and

Willson to use arbitrarily scaled bins as per Hsieh, since Hsieh decreases memory bandwidth required and provides numerous other benefits (see 2:20-40 and Abstract).

References Wilson and Willson do not expressly teach this limitation, whilst Reference Cloutier teaches in 7:28-40 specifically that a matrix of 8x4 PEs is implemented on each FPGAs where there is a 2x2 array of FPGAs in the first place, and Inada provides additional support. Given this, it would be reasonable to use a 4x4 array instead of an 8x4 array, given that each FPGA could easily be partitioned into a 4x4 array, as illustrated in Figure 3 anyway. Now, as set forth in the rejections to claims 1-3 above, the system of Cloutier is taught for use with image convolution, and further in Inada the use of interlaced scans is taught, such that the screen is divided up into units of say 4x4 pixels for faster drawing time. Therefore, if one FPGAs with a 4x4 array of PEs, or a 2x2 array of FPGAs with a 2x2 PE implementation, with each one dedicated processing a certain portion of the screen was used, and interleaving was used for the results, it would logical to use the claimed 4x4 architecture. Motivation and combination is taken from the parent claim and herein incorporated by reference, with additional motivation as set forth in the immediately preceding paragraph.

Claim 22 is rejected under 35 U.S.C. 103(a) as unpatentable over Wilson, Willson, and Inada as applied to claim 21 above, and further in view of Hsieh et al (US 6,819,321 B1).

As to claim 22, Inada clearly teaches dividing the screen into a plurality of bins but does not specifically teach sixteen sample managers and a four by four array of

bins. Reference Hsieh et al teaches dividing the screen into a number of bins for two-dimensional image processing, where the number can be arbitrary, but where an example given is four bins in Figure 4 (3:28-40). Applicant has not established any criticality to the number of sample managers and/or bins, and as such the choice of an arbitrary number of 'sample managers' or processing elements and the division of the screen into some arbitrary number of bins is a matter of design choice, see In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Inada, Wilson, and Willson to use arbitrarily scaled bins as per Hsieh, since Hsieh decreases memory bandwidth required and provides numerous other benefits (see 2:20-40 and Abstract).

Claims 23 is rejected under 35 U.S.C. 103(a) as unpatentable over Wilson, Willson, Inada, and Cloutier.

As to claim 23, this is a duplicate of claim 21, which is incorporated by reference, with the additional limitations from claim 5 above, the rejection to which is also incorporated by reference. Wilson uses groups of eight processors that can be configured into different exemplary configurations anyway, and Cloutier is dynamically reconfigurable as pointed out above. Also, Inada is **only** included for division of screen space, which examiner contends would be a notoriously and trivially obvious variant anyway.

Claim 24 is rejected under 35 U.S.C. 103(a) as unpatentable over Wilson, Willson, Cloutier, and Inada as applied to claim 3 above, and further in view of Hsieh et al (US 6,819,321 B1).

As to claim 24, Inada clearly teaches dividing the screen into a plurality of bins but does not specifically teach sixteen sample managers and a four by four array of bins. Reference Hsieh et al teaches dividing the screen into a number of bins for two-dimensional image processing, where the number can be arbitrary, but where an example given is four bins in Figure 4 (3:28-40). Applicant has not established any criticality to the number of sample managers and/or bins, and as such the choice of an arbitrary number of 'sample managers' or processing elements and the division of the screen into some arbitrary number of bins is a matter of design choice, see In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Inada, Wilson, and Willson, and Cloutier to use arbitrarily scaled bins as per Hsieh, since Hsieh decreases memory bandwidth required and provides numerous other benefits (see 2:20-40 and Abstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric V. Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 7:30-4:30 alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 571-272-7664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Woods

JEFFERY BRIER
PRIMARY EXAMINER

November 18, 2005